REMARKS

This amendment is responsive to the Office Action dated December 19, 2002. The title has been amended to reflect the elected claimed invention is only a method. Claims 1-16, and 33-44 are pending in this application. Claims 1-11, and 13-16 have been amended. Claim 12 is cancelled herein without prejudice. Claims 33-44 have been added. It is believed that no additional charges apply for supplemental claims, however, if necessary please charge Deposit Account No. 01-1960.

Claims 1-16 have been objected to for various informalities. Claims 1-11, 13 and 14 have been rejected under 35 U.S.C. §102(a) as being anticipated by Kwon et al., (US No. 6,235,552). Claims 12 and 15-16 have been objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

I. CLAIM OBJECTIONS

Claims 1-16 are objected to because they contain recitations without proper antecedent basis and other informalities. Claims 1-11, and 13-16 have been corrected to include the amendments suggested by the Examiner.

III. REJECTIONS UNDER 35 U.S.C. 102

Claims 1-3, 6 and 11 as best understood are rejected under 35. U.S.C. 102(a) as being anticipated by Kwon et al. In the first claim, Applicant's have taken the subject matter of cancelled claim 12 and incorporated it into claim 1. Particularly, the "thinning

of said pre-formed integrated circuit chip," is not disclosed in the prior art, as acknowledged by the Examiner.

Regarding claim 4, Examiner states that Kwon discloses the step of forming at least one test pad having gold on a conductive field metal. In doing so the Examiner cites Kwon, Col. 3, lines 14-33 and lines 44-48. However, within this text, no mention is made of gold conductive metals. In Col 3, line 50-54, the use of gold among other metals is mentioned, however this is for the chip pad and not the test pad of the interconnect assembly, as claimed.

Regarding claim 5, the Examiner rejected the limitation of this claim that included a plurality of stacked interconnect layers. In the rejection, the Examiner does not specifically cite subject matter disclosed in Kwon. Applicants respectfully submit, that Kwon does not disclose this matter, and that the limitation would be allowable if rewritten to include the limitations of the first independent claim. Therefore, Applicants have added independent claim 33, that included the subject matter of claims 1 and 5, and respectfully submit that this claim is allowable. Added claims 34-44, depend either directly or indirectly from claim 33 and should be allowable.

VI. SUMMARY

Based on the above amendments and accompanying remarks, Applicants respectfully submit that all pending claims are in condition for allowance and earnestly solicits a notice thereof. Applicant encourages the Examiner to telephone the undersigned attorney if it appears that a telephone conference would facilitate allowance of the application.

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on May 15, 2003
Angela Williams

Signature
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Version With Markings To Show Changes Made

In th Claims:

The claims have been amended as follows:

1. (Amended) A method of preparing a pre-formed integrated circuit chip for encapsulation in an electronic package, comprising the steps of:

forming an interconnect assembly separately from said pre-formed integrated circuit chip;

forming a plurality of conductive bumps connected to the terminals of the **pre-formed** integrated circuit chip;

bonding said interconnect assembly to said prepared integrated circuit chip; [and]

passivating said bonded interconnect assembly and said [prepared] **pre-formed** integrated circuit chip into an integral structure; **and**

thinning said pre-formed integrated circuit chip to provide said electronic package.

2. (Amended) The method of claim 1 wherein said step of forming [an] **said** interconnect assembly comprises forming said interconnect assembly on a releasable substrate.

3. (Amended) The method of claim 1 wherein said step of forming [an] **said** interconnect assembly comprises forming at least one test pad in an interconnect layer,

which at least one test pad can be accessed and electrically connected on opposing sides of said **at l ast on** test pad.

4. (Amended) The method of claim 3 wherein said step of forming at least one test pad forms a test pad having gold on [opposing sides of said test pad and sandwiched therebetween] a conductive field metal.

5. (Amended) The method of claim 3 wherein said step of forming [an] **said** interconnect assembly comprises forming at least one test pad in a plurality of stacked interconnect layers, each of which at least one test pad in each interconnect layer can be accessed and electrically connected on opposing sides of said **at least one** test pad.

6. (Amended) The method of claim 5 wherein said step of forming at least one test pad in [a] **said** plurality of stacked interconnect layers forms at least one test pad in each layer having gold on [opposing sides of said test pad and sandwiched therebetween] a conductive field metal.

7. (Amended) The method of claim 1 where said step of forming [a] **said** plurality of conductive bumps connected to the terminals of the integrated circuit chip [form] **forms** a metallic bump making connection to a terminal on said integrated circuit chip and a solder layer disposed on said metallic bump.

8. (Amended) The method of claim 7 wherein said step of forming [an] **said** interconnect assembly comprises forming at least one test pad in an interconnect layer, which at least one test pad can be accessed and electrically connected on opposing sides of said test pad, and wherein said step of bonding said interconnect assembly to said [prepared] **pre-formed** integrated circuit chip flip bonds said solder layer onto one side of said test pad.

9. (Amended) The method of claim 1 where said step of passivating said bonded interconnect assembly and said [prepared] **pre-formed** integrated circuit chip into [an] **said** integral structure to provide said electronic package comprises underfilling said pre-formed integrated circuit chip with an insulating material to remove all voids between said prepared integrated circuit chip and said interconnect assembly.

10. (Amended) The method of claim 1 where said step of passivating said bonded interconnect assembly and said [prepared] **pre-formed** integrated circuit chip into [an] **said** integral structure to provide said electronic package comprises potting said interconnect assembly and said pre-formed integrated circuit chip into an integral package.

11. (Amended) The method of claim 9 where said step of passivating said bonded interconnect assembly and said [prepared] **pre-formed** integrated circuit chip into [an] **said** integral structure to provide said electronic package comprises potting

said interconnect assembly and said pre-formed integrated circuit chip into said integral package.

13. (Amended) The method of claim 10 further comprising [the] **a** step of accessing said [prepared] **pre-formed** integrated circuit chip through electrical connection [said] to at least one test pad through a surface thereof opposing said surface of said **at least one** test pad contacting a terminal of said **pre-formed** integrated circuit chip to test said [prepared] **pre-formed** integrated circuit chip.

14. (Amended) The method of claim 10 and [wherein a] **further comprising a plurality of interconnect assembly and pre-formed integrated circuit chips wherein said** interconnect assembly and [prepared] **pre-formed** integrated circuit chips are bonded together to form a corresponding plurality of electronic packages and further comprising the step of releasing said plurality of electronic packages from each other.

15. (Amended) The method of claim 1 [wherein a] **further comprising a plurality of interconnect assembly and pre-formed integrated circuit chips wherein said** plurality of interconnect assembly and [prepared] **pre-formed** integrated circuit chips are bonded together to form a corresponding plurality of electronic packages and further comprising the step of testing said interconnect assembly and bonding a tested interconnect assembly in said step of bonding said interconnect assembly to said pre-formed integrated circuit chip only if said interconnect assembly tested good.

16. (Amended) The method of claim 15 where said step of forming said plurality of interconnect assemblies comprises forming said interconnect assemblies simultaneously in a wafer and where said plurality of [prepared] **pre-formed** integrated circuit chips are individually bump bonded to successfully tested ones of said interconnect assemblies.

33. A method of preparing a pre-formed integrated circuit chip for encapsulation in an electronic package, comprising the steps of:

forming an interconnect assembly separately from said pre-formed integrated circuit chip, said forming an interconnect assembly including the step of:

forming at least one test pad in a plurality of stacked interconnect layers, each of which at least one test pad in each interconnect layer can be accessed and electrically connected on opposing sides of said at least one test pad.

forming a plurality of conductive bumps connected to the terminals of the pre-formed integrated circuit chip;

bonding said interconnect assembly to said prepared integrated circuit chip; and

passivating said bonded interconnect assembly and said pre-formed integrated circuit chip into an integral structure to provide said electronic package.

34. The method of claim 33 wherein the at least one test pad has gold on a conductive field metal.

35. The method of claim 33 where said step of forming said plurality of conductive bumps connected to the terminals of the integrated circuit chip forms a metallic bump making connection to a terminal on said integrated circuit chip and a solder layer disposed on said metallic bump.

36. The method of claim 35 wherein said step of forming said interconnect assembly comprises forming at least one test pad in an interconnect layer, which at least one test pad can be accessed and electrically connected on opposing sides of said test pad, and wherein said step of bonding said interconnect assembly to said pre-formed integrated circuit chip flip bonds said solder layer onto one side of said test pad.

37. The method of claim 33 where said step of passivating said bonded interconnect assembly and said pre-formed integrated circuit chip into said integral structure to provide said electronic package comprises underfilling said pre-formed integrated circuit chip with an insulating material to remove all voids between said prepared integrated circuit chip and said interconnect assembly.

38. The method of claim 33 where said step of passivating said bonded interconnect assembly and said pre-formed integrated circuit chip into said integral structure to provide said electronic package comprises potting said interconnect assembly and said pre-formed integrated circuit chip into an integral package.

39. The method of claim 37 where said step of passivating said bonded interconnect assembly and said pre-formed integrated circuit chip into said integral structure to provide said electronic package comprises potting said interconnect assembly and said pre-formed integrated circuit chip into said integral package.

40. The method of claim 39 further comprising the step thinning said pre-formed integrated circuit chip.

41. The method of claim 39 further comprising a step of accessing said pre-formed integrated circuit chip through electrical connection to at least one test pad through a surface thereof opposing said surface of said at least one test pad contacting a terminal of said pre-formed integrated circuit chip to test said pre-formed integrated circuit chip.

42. The method of claim 39 and further comprising a plurality of interconnect assembly and pre-formed integrated circuit chips wherein said interconnect assembly and pre-formed integrated circuit chips are bonded together to form a corresponding plurality of electronic packages and further comprising the step of releasing said plurality of electronic packages from each other.

43. The method of claim 39 further comprising a plurality of interconnect assembly and pre-formed integrated circuit chips wherein said plurality of interconnect assembly and pre-formed integrated circuit chips are bonded together to form a corresponding plurality of electronic packages and further comprising the step of testing said interconnect assembly and bonding a tested interconnect assembly in said step of bonding said interconnect assembly to said pre-formed integrated circuit chip only if said interconnect assembly tested good.

44. The method of claim 43 where said step of forming said plurality of interconnect assemblies comprises forming said interconnect assemblies simultaneously in a wafer and where said plurality of pre-formed integrated circuit chips are individually bump bonded to successfully tested ones of said interconnect assemblies.